Ultrahigh Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

AC PERFORMANCE
- Gain Bandwidth Product: 1.4 GHz typ
- Unity Gain Bandwidth: 220 MHz typ
- High Slew Rate: 600 V/μs typ
- Full Power Response: 82 MHz typ
- Open-Loop Gain: 47 dB min, 52 dB typ

DC PERFORMANCE
- All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages
- V_{OS}: 5 mV max Over Full Temperature Range (AD5539S)
- I_B: 20 μA max (AD5539J)
- CMRR: 70 dB min, 85 dB typ
- PSRR: 100 μV/V typ
- MIL-STD-883B Parts Available

PRODUCT DESCRIPTION

The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

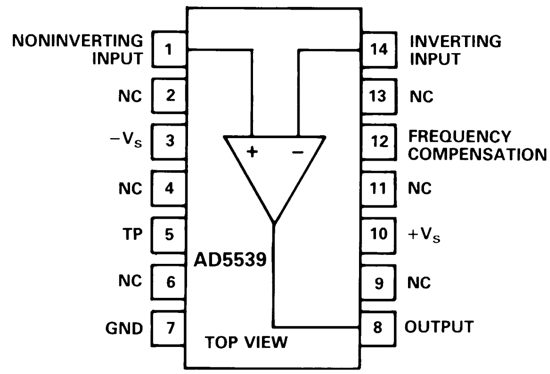
As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

CONNECTION DIAGRAM

Plastic DIP (N) Package or Cerdip (Q) Package



PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50 Ω and 75 Ω loads directly.
3. Input voltage noise is less than 4 nV$\sqrt{Hz}$.
4. Low cost RF and video speed performance.
5. ±2 volt output range into a 150 Ω load.
6. Low cost.
7. Chips available.

REV. B

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Tel: 617/329-4700 Fax: 617/326-8703

AD5539–SPECIFICATIONS (@ +25°C and V_S = ±8 V dc, unless otherwise noted)

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	**5**		2	**3**	mV
T_{MIN} to T_{MAX}			**6**			**5**	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	**2**		0.1	**1**	µA
T_{MIN} to T_{MAX}			**5**			**3**	µA
INPUT BIAS CURRENT							
Initial[2]							
V_{CM} = 0		6	**20**		6	**13**	µA
Either Input							
T_{MIN} to T_{MAX}			**40**			**25**	µA
FREQUENCY RESPONSE							
R_L = 150 Ω[3]							
Small Signal Bandwidth		220			220		MHz
A_{CL} = 2[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26 dB							
Full Power Response							
A_{CL} = 2[4]		68			68		MHz
A_{CL} = 7		82			82		MHz
A_{CL} = 20		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/µs
Large Signal Propagation Delay		4			4		ns
Total Harmonic Distortion							
R_L = ∞		0.010			0.010		%
R_L = 100 Ω[3]		0.016			0.016		%
V_{OUT} = 2 V p–p							
A_{CL} = 7, f = 1 kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f <10 MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common-Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common-Mode Rejection Ratio							
ΔV_{CM} = 1.7 V							
R_S = 100 Ω	**70**	85		**70**	85		dB
T_{MIN} to T_{MAX}	**60**			**60**			dB
INPUT VOLTAGE NOISE							
Wideband RMS Noise (RTI)		5			5		FV
BW = 5 MHz; R_S = 50 Ω							
Spot Noise		4			4		nV√Hz
F = 1 kHz; R_S = 50 Ω							
OPEN-LOOP GAIN							
V_O = +2.3 V, –1.7 V							
R_L = 150 Ω[3]	**47**	52	**58**	**47**	52	**58**	dB
R_L = 2 kΩ	**47**		**58**	**48**		**57**	dB
T_{MIN} to T_{MAX} –R_L = 2 kΩ	**43**		**63**	**46**		**60**	dB

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
OUTPUT CHARACTERISTICS							
Positive Output Swing							
R_L = 150 Ω[3]	+2.3	+2.8		+2.3	+2.8		V
R_L = 2 kΩ	+2.3	+3.3		+2.5	+3.3		V
T_{MIN} to T_{MAX} with R_L = 2 kΩ	+2.3			+2.3			V
Negative Output Swing							
R_L = 150 Ω[3]		–2.2	**–1.7**		–2.2	**–1.7**	V
R_L = 2 kΩ		–2.9	**–1.7**		–2.9	**–2.0**	V
T_{MIN} to T_{MAX} with R_L = 2 kΩ			**–1.5**			**–1.5**	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	**±4.5**		**±10**	**±4.5**		**±10**	V
Quiescent Current							
Initial I_{CC}+		14	**18**		14	**17**	mA
T_{MIN} to T_{MAX}			**20**			**18**	mA
Initial I_{CC}–		11	**15**		11	**14**	mA
T_{MIN} to T_{MAX}			**17**			**15**	mA
PSRR							
Initial		100	**1000**		100	**1000**	µV/V
T_{MIN} to T_{MAX}			**2000**			**2000**	µV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0°C to +70°C)	AD5539JN, AD5539JQ						
Military (–55°C to +125°C)					AD5539SQ		
PACKAGE OPTIONS							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ, AD5539SQ/883B			
J and S Grade Chips Available							

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]R_X = 470 Ω to $-V_S$.

[4]Externally compensated.

[5]Defined as voltage between inputs, such that neither exceeds +2.5 V, –5.0 V from ground.

Specifications subject to change without notice.

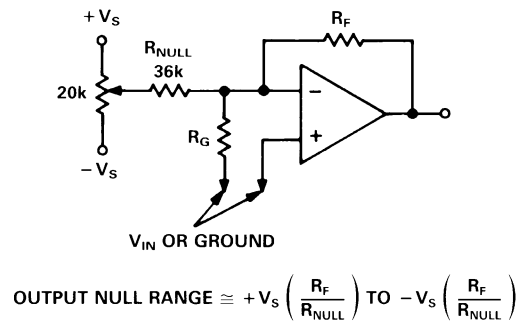
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	±10 V
Internal Power Dissipation	550 mW
Input Voltage	+2.5 V, –5.0 V
Differential Input Voltage	0.25 V
Storage Temperature Range (Q)	–65°C to +150°C
Storage Temperature Range (N)	–65°C to +125°C
Operating Temperature Range	
AD5539JN	0°C to +70°C
AD5539JQ	0°C to +70°C
AD5539SQ	–55°C to +125°C
Lead Temperature Range (Soldering 60 Seconds)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

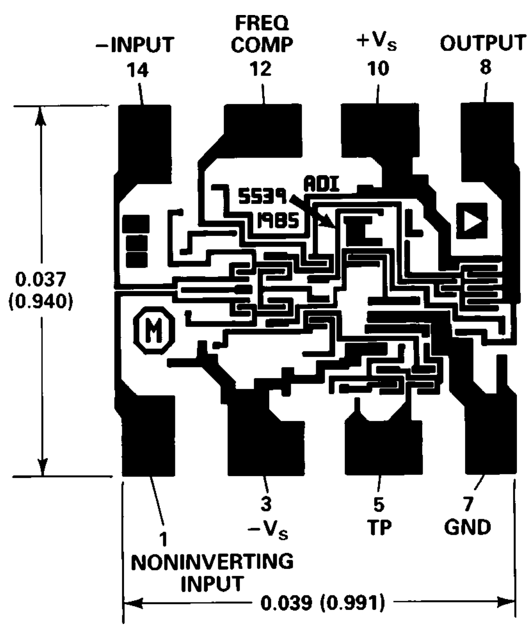
OFFSET NULL CONFIGURATION



OFFSET NULL CONFIGURATION

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5539 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



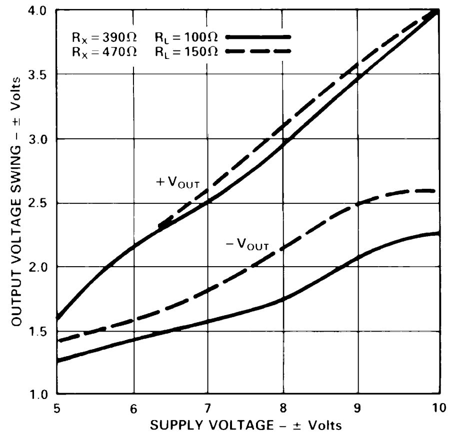


Figure 1. Output Voltage Swing vs. Supply Voltage

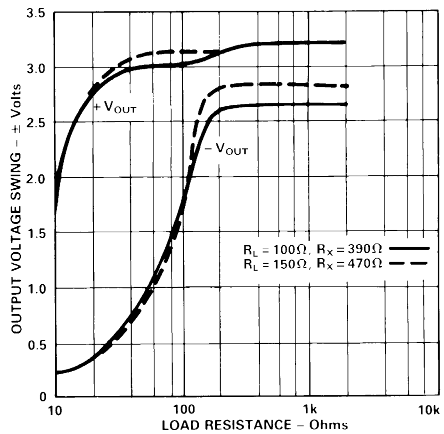


Figure 2. Output Voltage Swing vs. Load Resistance

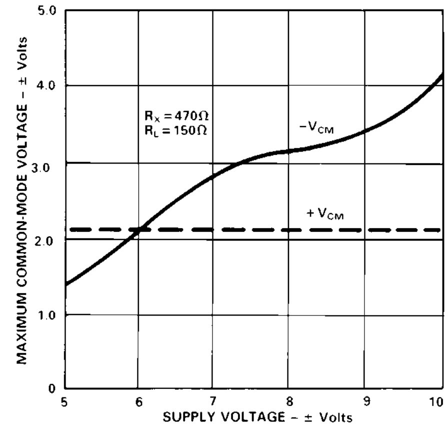


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

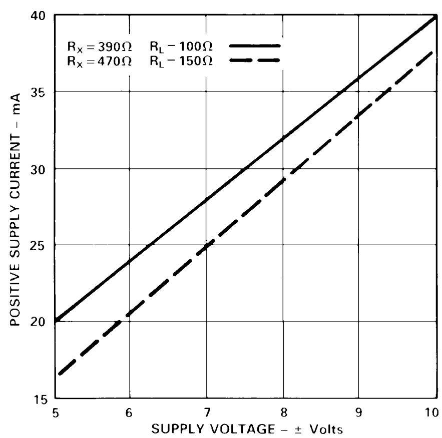


Figure 4. Positive Supply Current vs. Supply Voltage

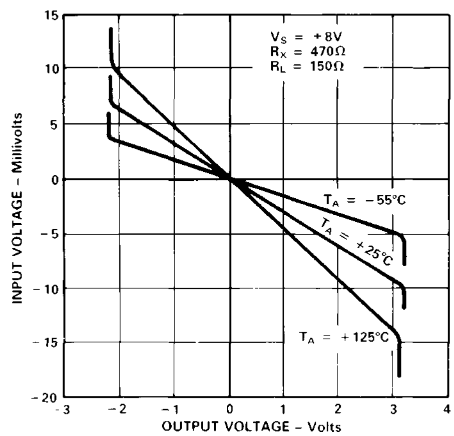


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

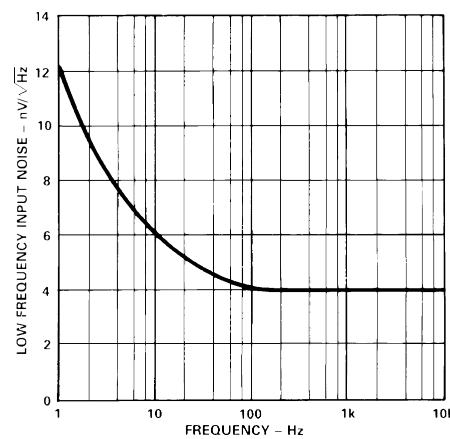


Figure 6. Low Frequency Input Noise vs. Frequency

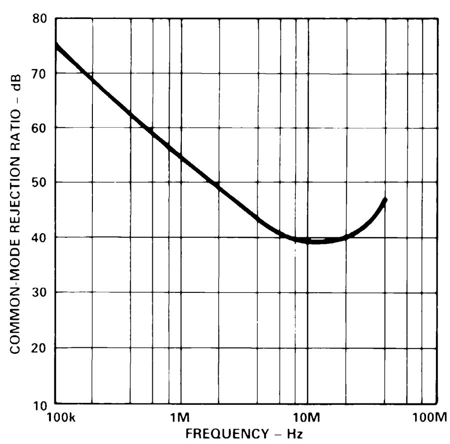


Figure 7. Common-Mode Rejection Ratio vs. Frequency

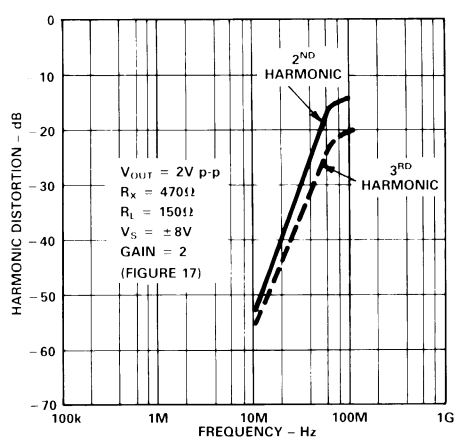


Figure 8. Harmonic Distortion vs. Frequency – Low Gain

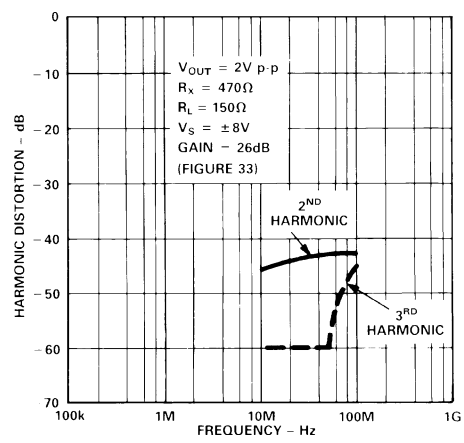


Figure 9. Harmonic Distortion vs. Frequency – High Gain

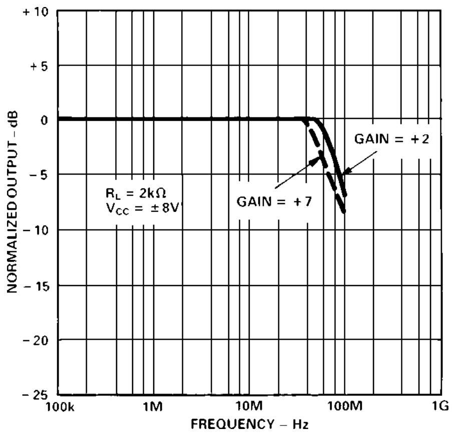


Figure 10. Full Power Response

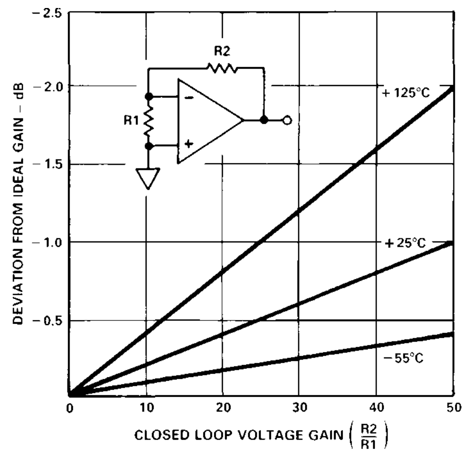


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

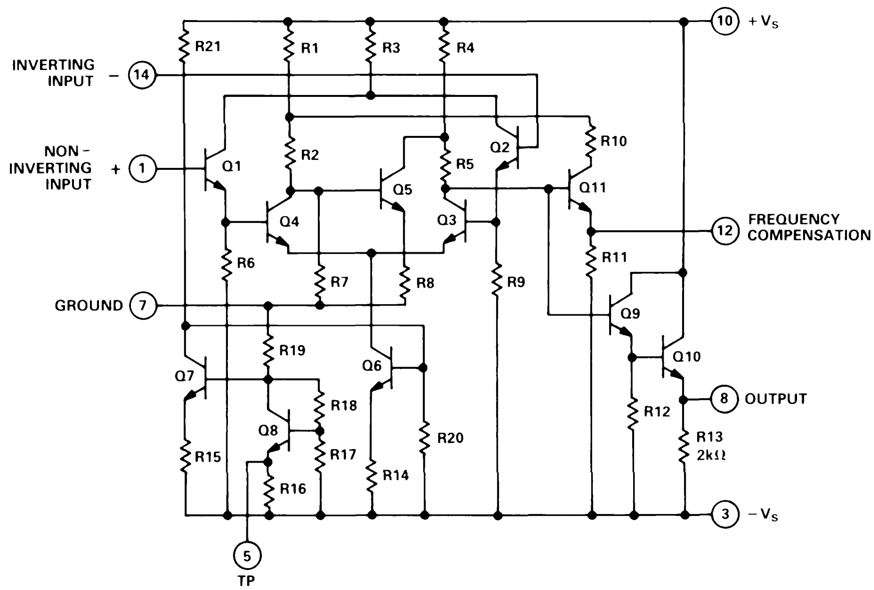


Figure 12. AD5539 Circuit

FUNCTIONAL DESCRIPTION

The AD5539 is a two-stage, very high frequency amplifier. Darlington input transistors Q1, Q4–Q2, Q3 form the first stage—a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is then summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned, via a small resistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a Darlington voltage follower with a resistive pull-down. The bias section, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

SOME GENERAL PRINCIPLES OF HIGH FREQUENCY CIRCUIT DESIGN

In designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved, some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50 Ω line for telecommunications purposes and 75 Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6 dB), adequate for many applications.

All of the circuits here were built and tested in a 50 Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small signal frequency response as those shown in this data sheet.

APPLYING THE AD5539

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding –3 dB bandwidths up to 390 MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation) so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44 MHz, independent of signal gain.

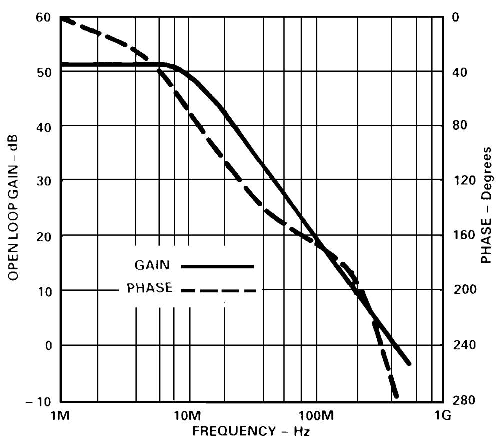


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10 MHz (see Figure 13). At frequencies beyond 100 MHz, phase shift increases such that the output lags the input by 180°—well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539

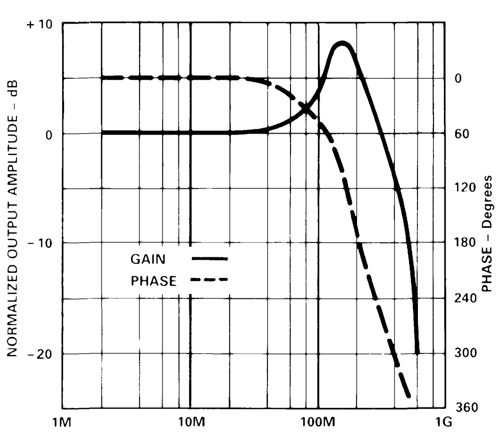


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10 dB of peaking at 150 MHz.

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high frequency response. The stray capacitance between the amplifier summing junction and ground, C_X, represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring R_{LAG} and C_{LAG} for now): the feedback network, consisting of R2 and C_{LEAD}, has a pole frequency equal to:

$$F_A = \frac{1}{2\pi\left(C_{LEAD} + C_X\right)\left(R1 \| R2\right)} \tag{1}$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi\left(R1 \times C_{LEAD}\right)} \tag{2}$$

Usually, frequency F_A is made equal to F_B; that is, $(R1C_X) = (R2\ C_{LEAD})$, in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency, F_A, will lie above the unity gain crossover frequency (440 MHz), then the optimum location of F_B will be near the crossover

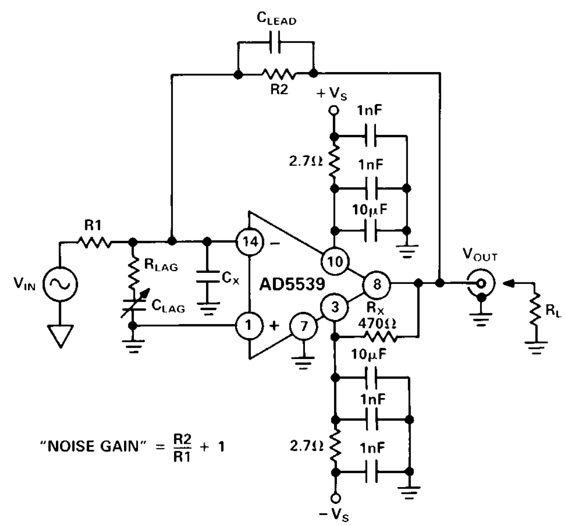


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

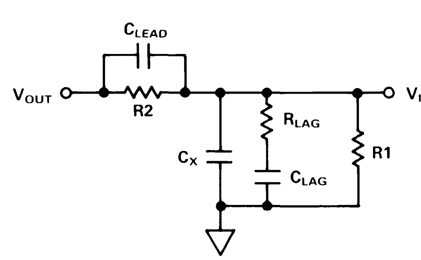


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

frequency. Both of these circuit techniques add a large amount of leading phase shift at the crossover frequency, greatly aiding stability.

The lag network (R_{LAG}, C_{LAG}) increases the feedback attenuation, i.e., the amplifier operates at a higher noise gain, above some frequency, typically one-tenth of the crossover frequency. As an example, to achieve a noise gain of 5 at frequencies above 44 MHz, for the circuit of Figure 15, would require a network of:

$$R_{LAG} = \frac{R1}{\left(4R1/R2\right) - 1} \tag{3}$$

and . . .

$$C_{LAG} = \frac{1}{2\,\pi\,R_{LAG}\left(44 \times 10^{6}\right)} \tag{4}$$

It is worth noting that an R_{LAG} resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

SOME PRACTICAL CIRCUITS

The preceding general principles may now be applied to some actual circuits.

A General Purpose Inverter Circuit

Figure 17 is a general purpose inverter circuit operating at a gain of –2.

For this circuit, the total capacitance at the inverting input is approximately 3 pF; therefore, C_{LEAD} from Equations 1 and 2 needs to be approximately 1.5 pF. As shown in Figure 17, a small trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within ±0.5 dB to 170 MHz and the –3 dB bandwidth is 200 MHz.

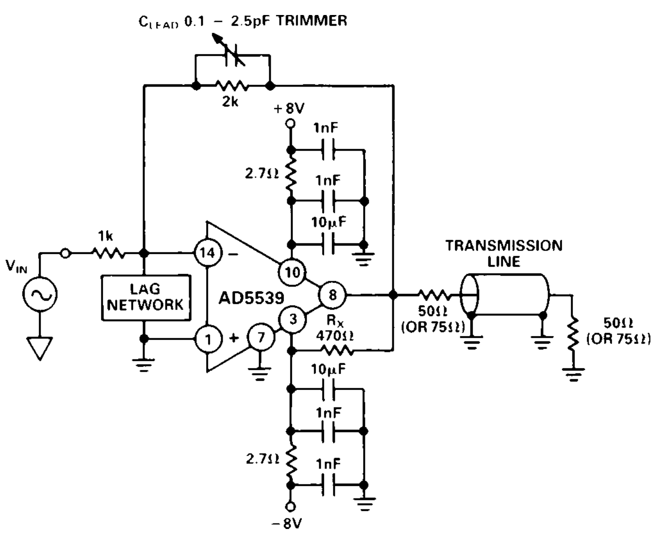


Figure 17. A General Purpose Inverter Circuit

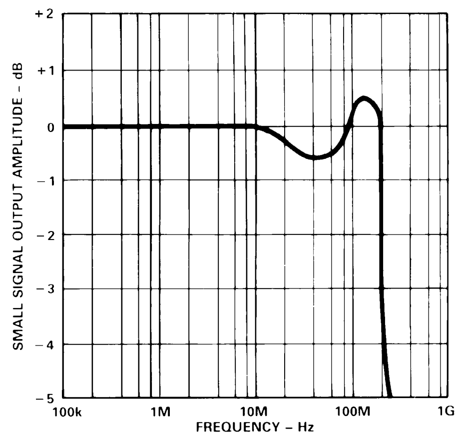


Figure 18. Response of the (Figure 17) Inverter Circuit without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor C_{LEAD} adjustable; in some cases, C_{LAG} must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

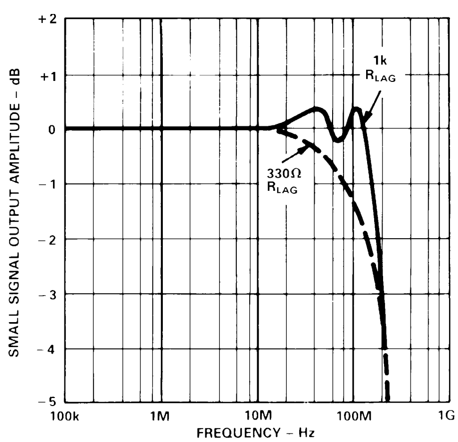


Figure 19. Response of the (Figure 17) Inverter Circuit with an R_{LAG} Compensation Network Employed

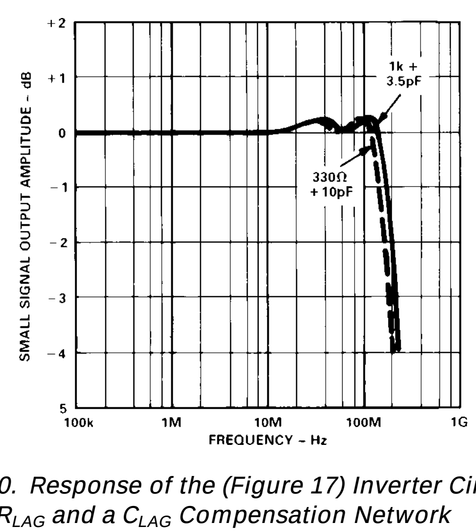


Figure 20. Response of the (Figure 17) Inverter Circuit with an R_{LAG} and a C_{LAG} Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with C_{LEAD} = 1.5 pF, R_{LAG} = 330 Ω and C_{LAG} = 3.5 pF.

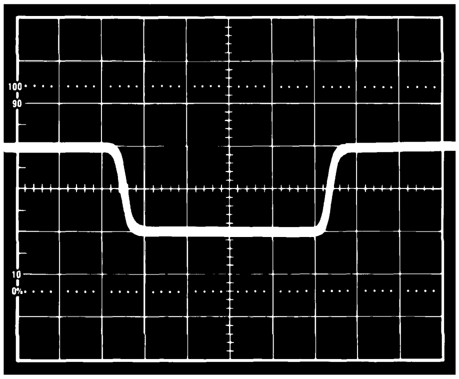


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

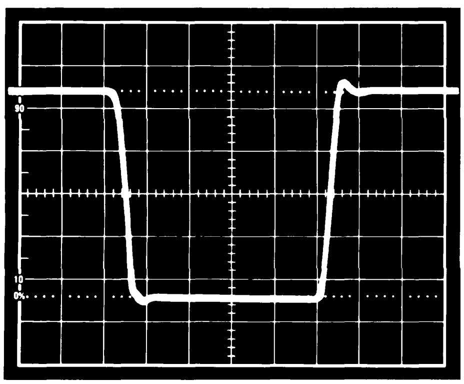


Figure 22. Large Signal Response of the (Figure 17) Inverter Circuit; Vertical Scale: 200 mV/div, Horizontal Scale: 5 ns/div

A C_{LEAD} capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$$\left(-3\,dB\ \ frequency = \frac{1}{2\,\pi\,R2\,C_{LEAD}} \right)$$

If this option is selected, it is recommended that a C_{LEAD} be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350 MHz) which would otherwise occur when using the circuit of Figure 17 with a C_{LEAD} of more than about 2 pF.

Figure 24 shows the response of the circuit of Figure 23 for each connection of C_{LEAD}. Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting C_{LEAD} directly to the output, as was done in Figure 17.

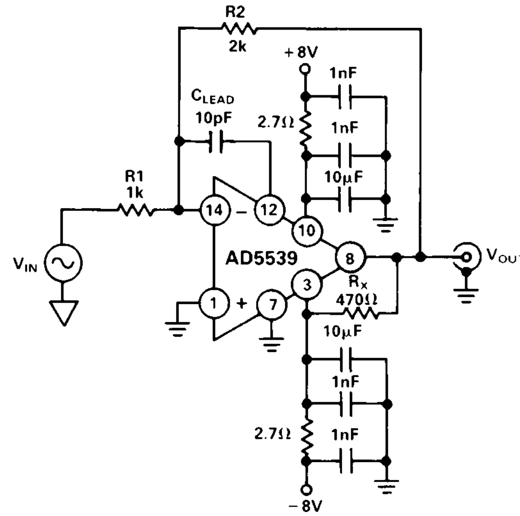


Figure 23. A Gain of 2 Inverter Circuit with the C_{LEAD} Capacitor Connected to Pin 12

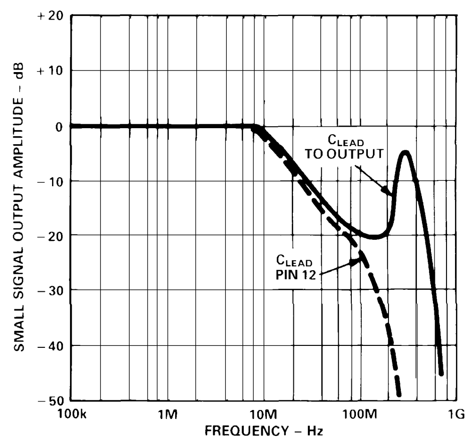


Figure 24. Response of the Circuit of Figure 23 with C_{LEAD} = 10 pF

A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with C_{LEAD} connected normally (across the feedback resistor – Figure 25) will require a source resistance of 200 Ω or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest –3 dB frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

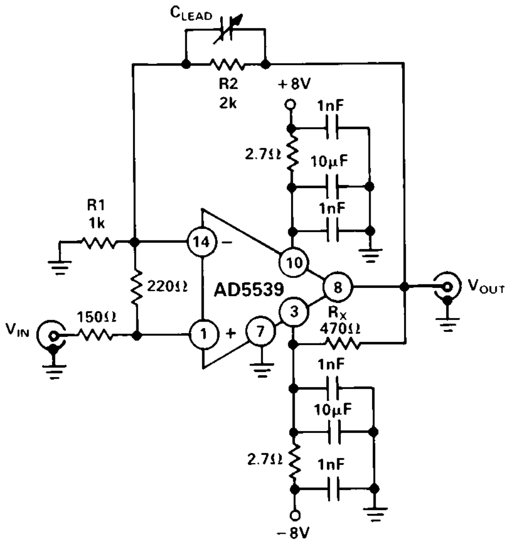


Figure 25. A Gain of 3 Follower with Both Lead and Lag Compensation

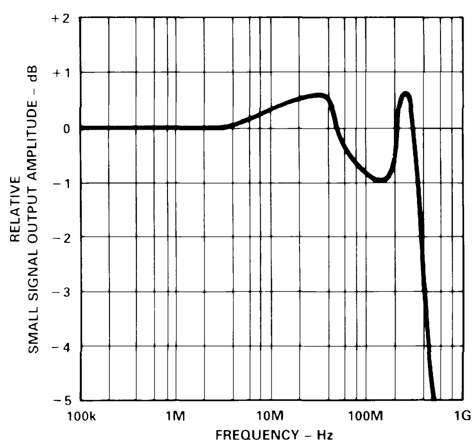


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the midband and low frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

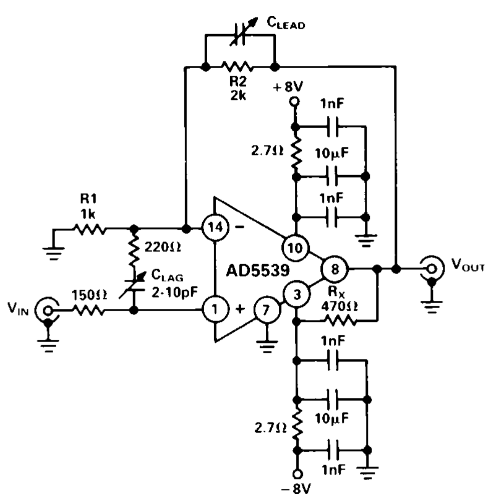


Figure 27. A Gain of 3 Follower Circuit with Both C_{LEAD} and R_{LAG} Compensation

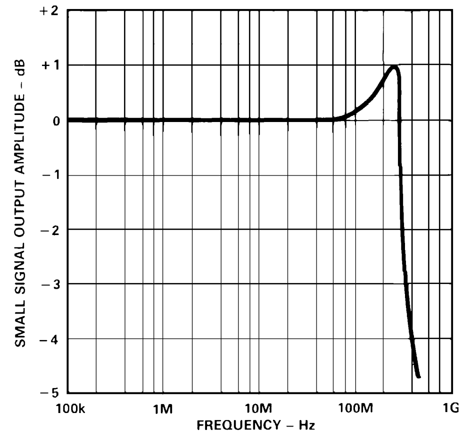


Figure 28. Response of the Gain of 3 Follower with C_{LEAD}, C_{LAG} and R_{LAG}

These same principles may be applied when capacitor C_{LEAD} is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of R_{LAG}. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the

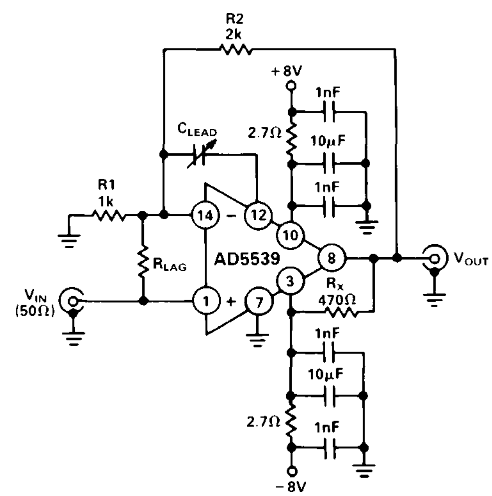


Figure 29. A Gain of 3 Follower Circuit with C_{LEAD} Compensation Connected to Pin 12

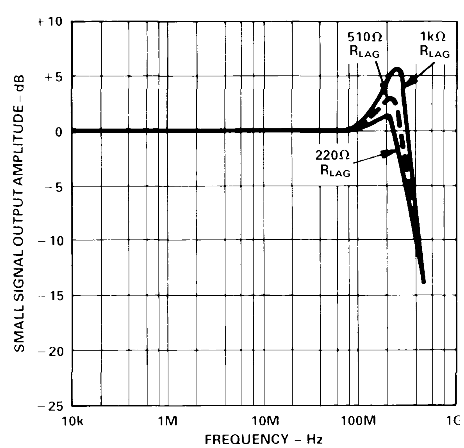


Figure 30. Response of the Gain of 3 Follower Circuit with C_{LEAD} Connected to Pin 12

value of R_{LAG}, the higher the noise gain). For example, with a 220 Ω R_{LAG} and a 50 Ω source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

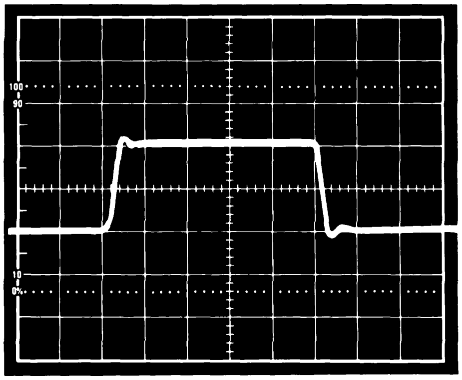


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

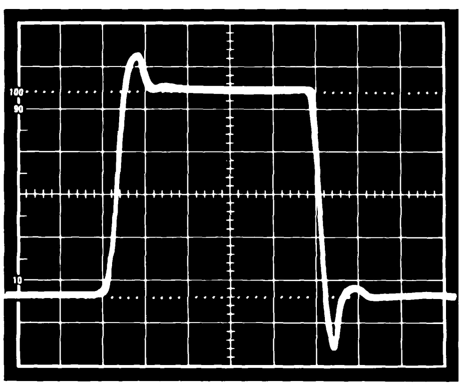


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

A Video Amplifier Circuit with 20 dB Gain (Terminated)
High gain applications (14 dB and up) require only a small lead capacitance to obtain flat response. The 26 dB (20 dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5-1 pF lead capacitance. Again, a small C_{LEAD} can be connected, either to the output or to Pin 12 with very little difference in response.

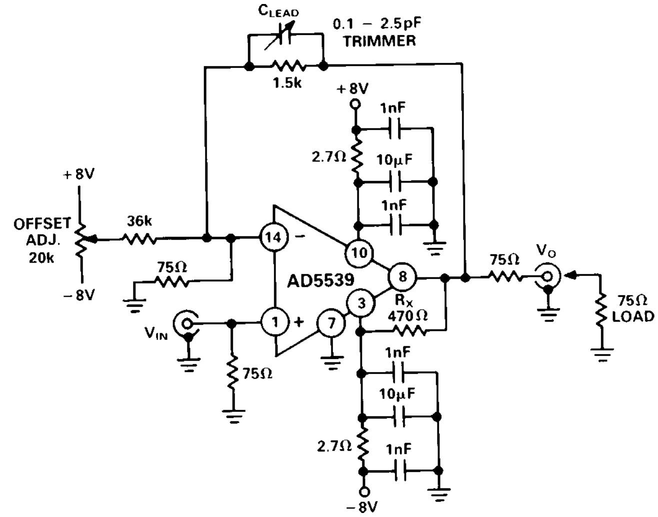


Figure 33. A 20 dB Gain Video Amplifier for 75 Ω Systems

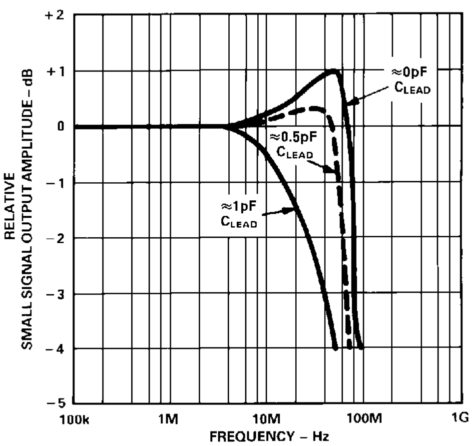


Figure 34. Response of the 20 dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35 and 36 show a circuit and test setup to measure the AD5539's response to a modulated ramp signal (0-90 IRE p-p ramp, 40 IRE p-p modulation, 4.4 MHz).

Figures 37 and 38 show the differential gain and phase response.

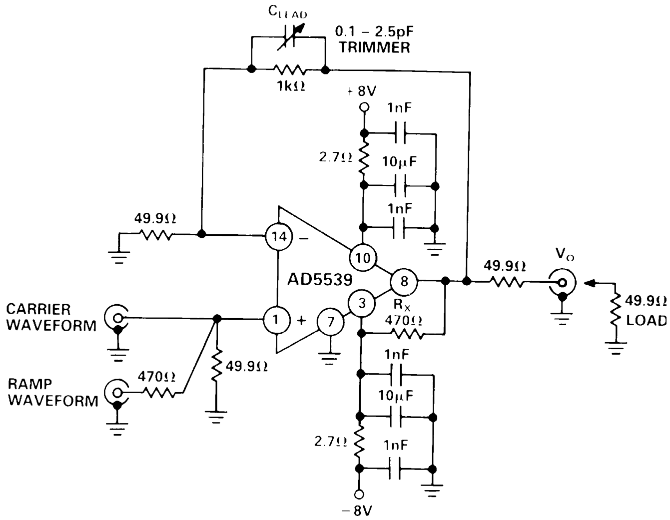


Figure 35. Differential Gain and Phase Measurement Circuit

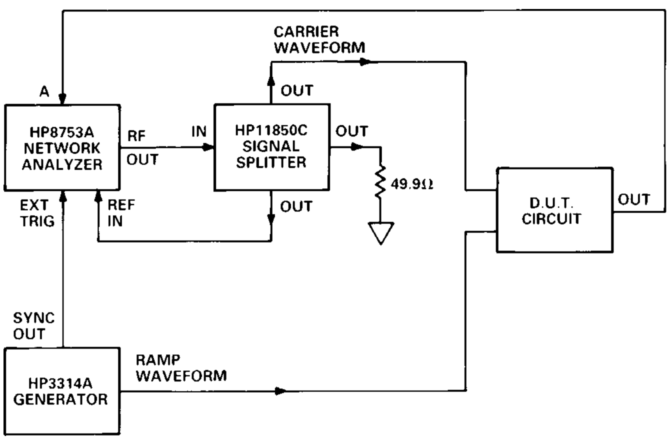


Figure 36. Differential Gain and Phase Test Setup

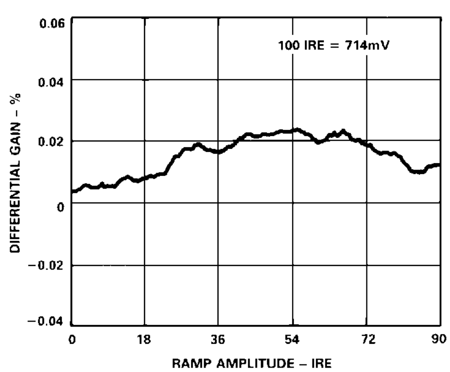


Figure 37. Differential Gain vs. Ramp Amplitude

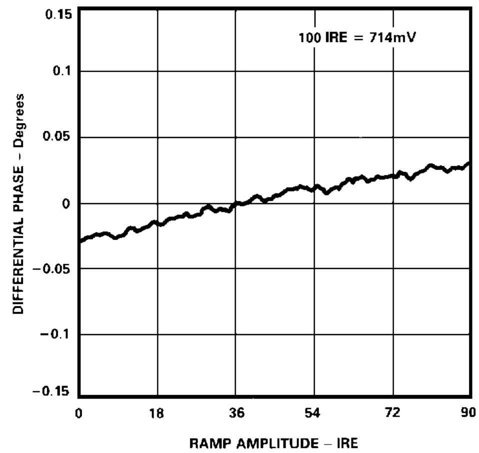


Figure 38. Differential Phase vs. Ramp Amplitude

MEASURING AD5539 SETTLING TIME

Measuring the very rapid settling times associated with AD5539 can be a real problem for the designer; proper component layout must be used and appropriate test equipment selected. In addition, both cable dispersion (a function of cable losses) and the quality of termination (SWR) directly affect the measurement. The circuit of Figure 39 was used to make a "brute force" AD5539 settling time measurement. The fixture containing the circuit was connected directly—using a male BNC connector (but no cable)—onto the front of a 50 Ω input oscilloscope preamp. A digital mainframe was then used to capture, average, and expand the error signal. Most of the small-scale waveform aberrations shown on the figure were caused by the oscilloscope itself, especially the glitch at 15 ns. The pulse source used for this measurement was an EH-SPG2000 pulse generator set for a 1 ns rise-time; it was coupled directly to the circuit using 18" of microwave 50 Ω hard line.

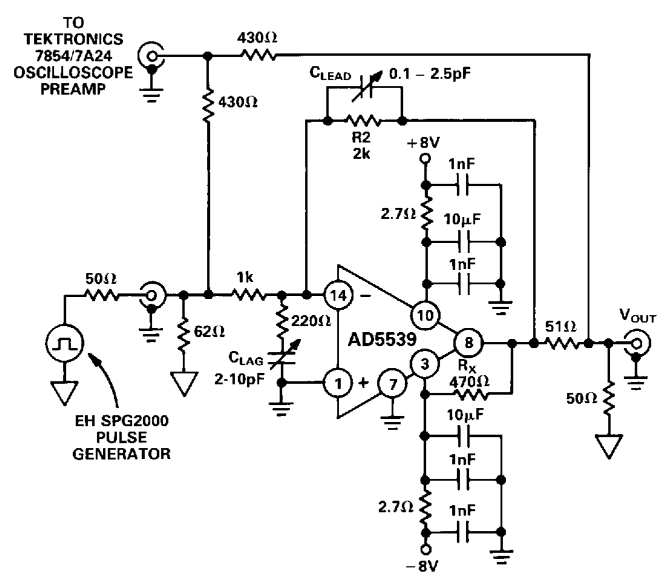


Figure 39. AD5539 Settling Time Test Circuit

APPLICATIONS SUMMARY CHART

	R1	R2[1]	R_{LAG}	C_{LAG}[2]	C_{LEAD}[2]	GAIN	GAIN FLATNESS (TRIMMED)	3 dB BANDWIDTH
Gain = –1 to –5 Circuit of Fig. 17	$\frac{R2}{G}$	2 k	$\leq \frac{R1}{4\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi\left(44\times 10^{6}\right)R_{LAG}}$	$\approx \frac{3pF}{G}$	–2	±0.2 dB	200 MHz
Gain = –1 to –5 Circuit of Fig. 23	$\frac{R2}{G}$	2 k	$\leq \frac{R1}{4\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi\left(44\times 10^{6}\right)R_{LAG}}$	$\approx \frac{3pF}{G}$	–2	±1 dB	180 MHz
Gain = +2 to +5[3] Circuit of Fig. 27	$\frac{R2}{G-1}$	2 k	$\leq \frac{R1}{10\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi\left(44\times 10^{6}\right)R_{LAG}}$	$\approx \frac{3pF}{G-1}$	+3	±1 dB	390 MHz
Gain = +2 to +5[4] Circuit of Fig. 29	$\frac{R2}{G-1}$	2 k	$\leq \frac{R1}{10\frac{R1}{R2}-1}$	NA	$\approx \frac{3pF}{G-1}$	+3	±0.5 dB	340 MHz
Gain < –5	$\frac{R2}{G}$	1.5 k	NA	NA	Trimmer[5]	–20	±0.2 dB	80 MHz
Gain > +5	$\frac{R2}{G-1}$	1.5 k	NA	NA	Trimmer[5]	+20	±0.2 dB	80 MHz

NOTES
G = Gain NA = Not Applicable
[1]Values given for specific results summarized here—applications can be adapted for values different than those specified.
[2]It is recommended that C_{LEAD} and C_{LAG} be trimmers covering a range that includes the computed value above.
[3]$R_{SOURCE} \geq 200\ \Omega$.
[4]$R_{SOURCE} \geq 50\ \Omega$.
[5]Use Voltronics CPA2 0.1–2.5 pF Teflon Trimmer Capacitor (or equivalent).

The photos of Figures 40 and 41 demonstrate how the AD5539 easily settles to 1% (1 mV) in less than 12 ns; settling to 0.1% (100 µV) requires less than 25 ns.

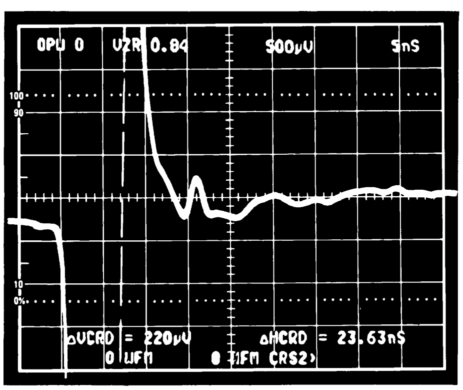


Figure 40. Error Signal from AD5539 Settling Time Test Circuit – Falling Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 µV/div

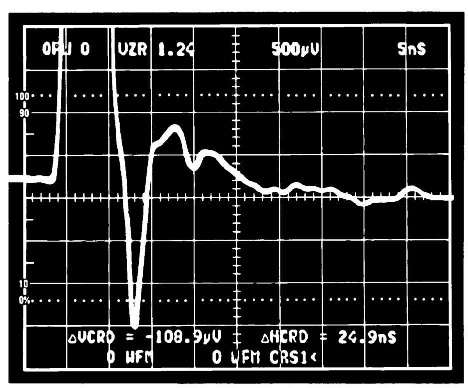


Figure 41. Error Signal from AD5539 Settling Time Test Circuit – Rising Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 µV/div

Figure 42 shows the oscilloscope response of the generator alone, set up to simulate the ideal test circuit error signal (Figure 43).

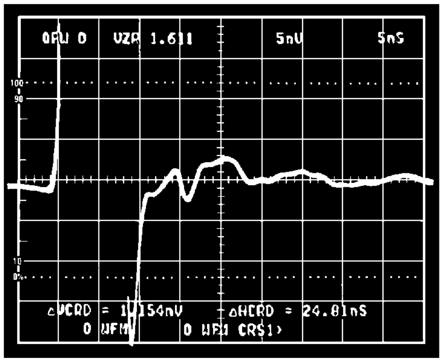


Figure 42. The Oscilloscope Response Alone Directly Driven by the Test Generator. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

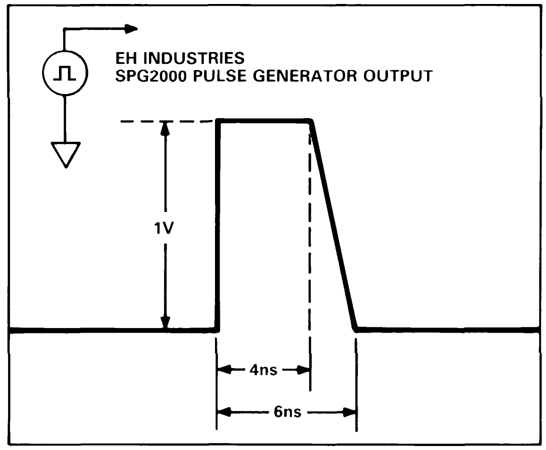


Figure 43. A Simulated Ideal Test Circuit Error Signal

A 50 MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 44 is a circuit for a 50 MHz voltage-controlled amplifier (VCA) suitable for use in high quality video-speed applications. This circuit uses the AD5539 as an output amplifier for the AD539, a high bandwidth multiplier. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven ($V_X < 0$ or $V_X > 3.3$ V). Secondly, it provides a choice of either noninverting or inverting responses, using either input V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT} = \frac{V_X\left(V_{Y1-}V_{Y2}\right)}{2V} \text{ for } V_X > 0$$

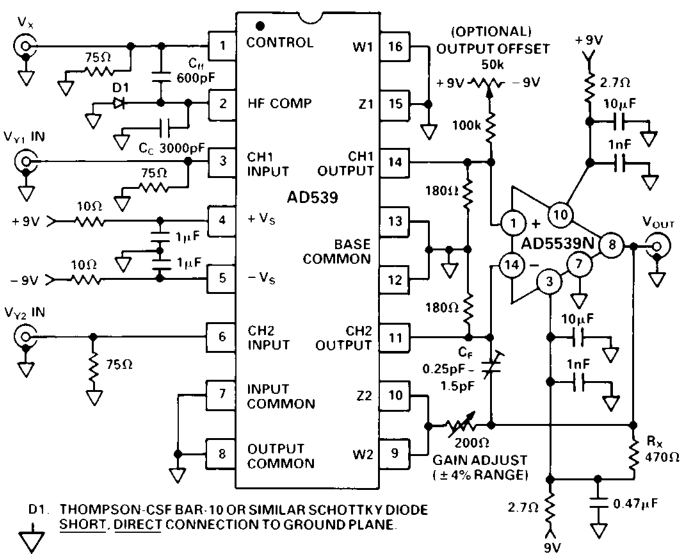


Figure 44. A Wide Bandwidth Voltage-Controlled Amplifier

Hence, the gain is unity at V_X = +2 V. Since V_X can overrange to +3.3 V, the maximum gain in this configuration is about 4.3 dB. (Note: If Pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10 dB.)

The bandwidth of this circuit is over 50 MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, extreme care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 45 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: V_{Y1} = 0.5 V rms for values of V_X from +10 mV to +3.16 V; this is with a 75 Ω load on the output. The feedthrough at V_X = –10 mV is also shown.

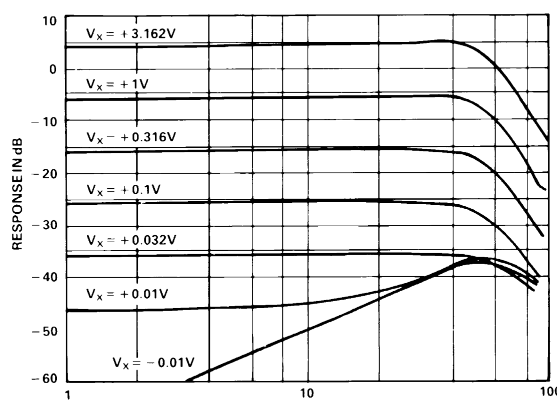


Figure 45. AC Response of the VCA at Different Gains V_Y = 0.5 V RMS

The transient response of the signal channel at V_X = +2 V, V_Y = V_{OUT} = + or –1 V is shown in Figure 46; with the VCA driving a 75 Ω load. The rise and fall times are both approximately 7 ns.

A few final circuit details: in general, the control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000 pF (3 nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1 µF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal.

The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2 MHz with a C_C of 0.01 µF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (Pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

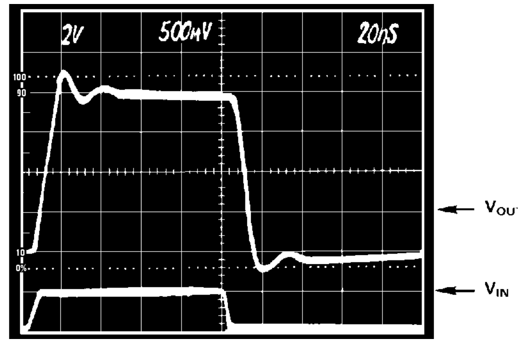


Figure 46. Transient Response of the Voltage-Controlled Amplifier V_X = +2 Volts, V_Y = ±1 Volt

Diode D1 clamps the logarithmic control node at Pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 47 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high fre-

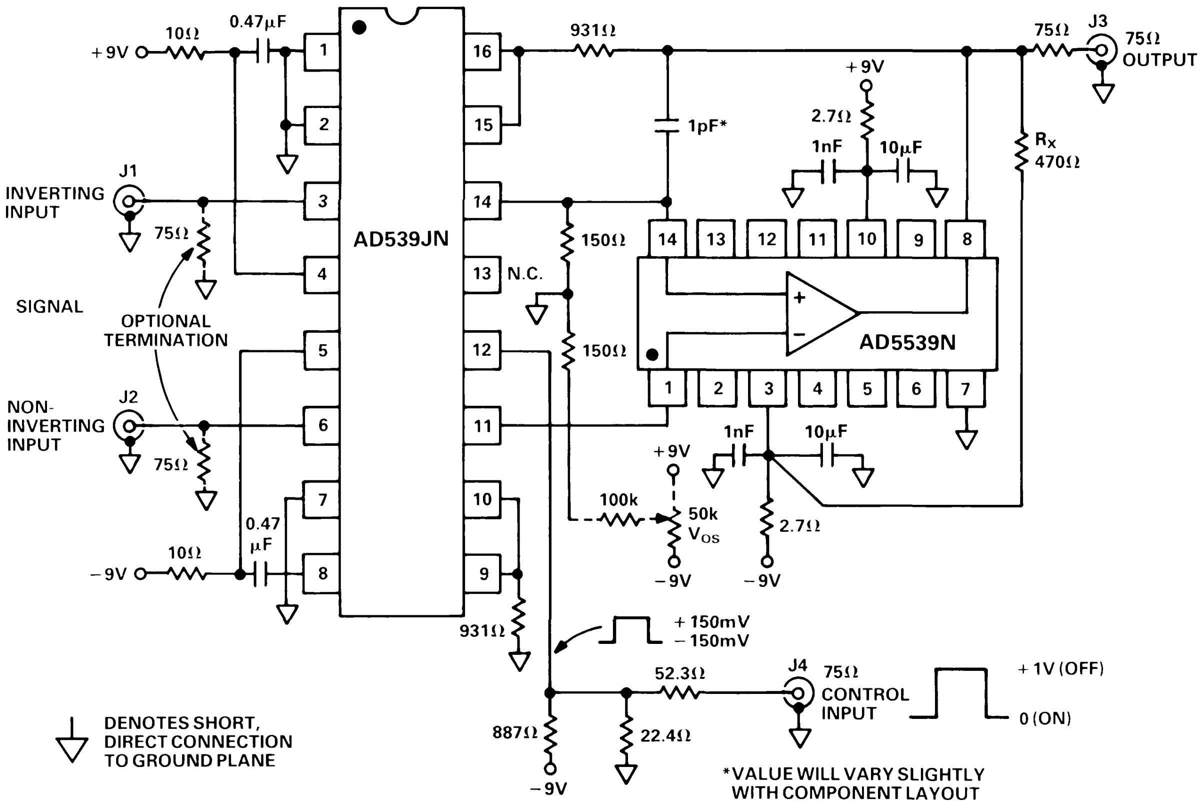


Figure 47. An Analog Multiplier Video Switch

quency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1 V into a reverse-terminated 75 Ω load (or ±2 V into 150 Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1 V at either input generates ±1 V (noninverting) or ∓1 V (inverting) across the 75 Ω load. The circuit provides a gain of about 1, when "ON," or zero when "OFF."

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step changes in the output current as the AD539 is gated on or off.

Figure 49 shows the response to a pulse of 0 to +1 V on the signal channel. With the control input held at zero, the rise time is under 10 ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05 dB over a signal window of 0 to +1 V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58 MHz. The noise level of this circuit measured at the 75 Ω load is typically 200 μV in a 0 MHz to 5 MHz bandwidth or approximately 100 nV per root hertz. The noise spectral density is essentially flat to 40 MHz.

The waveforms shown in Figures 48 and 49 were taken across a 75 Ω termination; in both photos, the signal of 0 to +1 V (in this case, an offset sine wave at 1 MHz) was applied to the noninverting input. In Figure 48, the envelope response shows the output being fully switched in about 50 ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1 V or more. There is very little control-signal breakthrough.

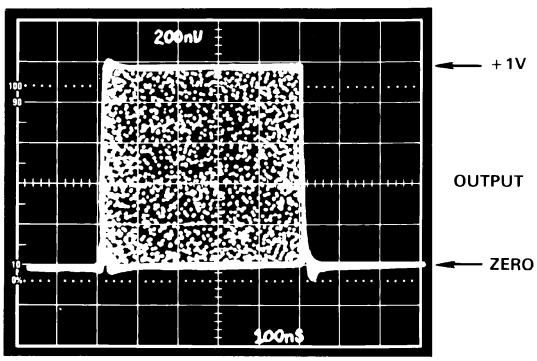


Figure 48. The Control Response of the Video Switcher

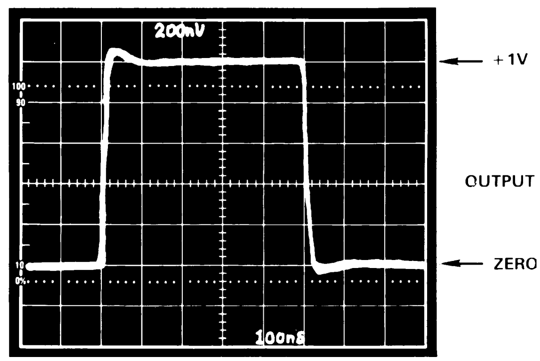
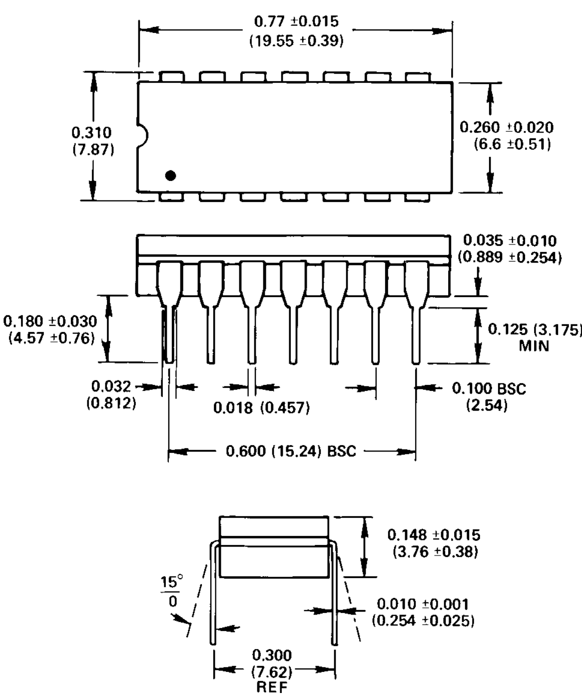


Figure 49. The Signal Response of the Video Switcher

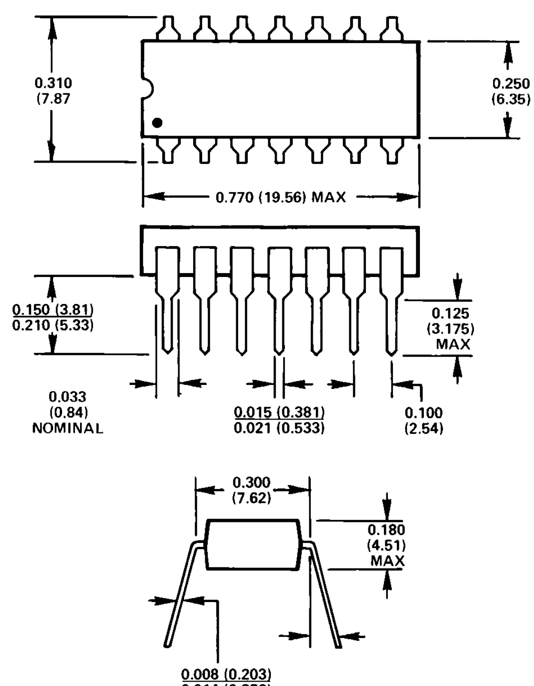
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Pin Cerdip Package (Q-14)



14-Pin Plastic DIP Package (N-14)



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